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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/894,062	06/28/2001	Hong-Kyu Kim	8836-136 (IB10137-US)	5463

7590 11/05/2003

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EXAMINER	
LANEAU, RONALD	
ART UNIT	**PAPER NUMBER**
2674	2

DATE MAILED: 11/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/894,062	KIM ET AL.	
	Examiner	Art Unit	
	Ronald Laneau	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7 and 8* is/are rejected.

7)☒ Claim(s) *4-6 and 9-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 7, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over Ishii et al (US 6,288,698) in view of Hinman et al (US 4,819,190).

As per claims 1, Ishii et al teach a liquid crystal display (LCD) controller 10 generating control signals for displaying in response to pixel data to display pictures on a liquid crystal panel having a plurality of pixels comprising a dithering pattern register section for storing binary data of gray levels, wherein a certain number of gray levels have a same bit number as denominator values of certain number of gray levels (col. 4, lines 1-5 and 48-64, figs. 6A, 6B); multiplexers for generating data patterns for the respective gray levels in accordance with an

output of the respective modular register counters; and a selection means 13 for selecting and generating a corresponding bit of a data pattern corresponding to the pixel data provided on a LCD panel among the data patterns (col. 5, lines 14-30). Ishii et al do not teach modular register counters for performing counting operation to determine a binary value of most significant bit of each of the gray levels in response to a frame clock, a line clock, and a pixel clock but Hinman et al teach a pixel counter which equivalent to the modular register counter 181 which is incremented every pixel time by pixel clock 171 which is reset every frame by line clock 175, and a line counter 182 which is incremented every video line and is reset every frame by a frame clock 176 (col. 7, lines 55-59).

It would have been obvious to one of ordinary skill in the art to utilize the pixel counter as taught by Hinman et al into the device of Ishii et al because it would provide great accuracy in determining the bit values and at the same time improve the display quality.

As per claim 7, Hinman et al teach a liquid crystal display wherein the modular frame counter, the modular line counter, and the modular pixel counter are initialized to a predetermined value whenever the frame is changed, the line is changed, and the pixel is changed, respectively (col. 7, lines 55-59).

As per claim 8, this is a method claim corresponding to the apparatus of claim 1 and is therefore rejected on the same basis as claim 1.

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over as being unpatentable over Ishii et al (US 6,288,698) in view of Weise et al (US 5,638,187).

As per claim 2, Ishii et al do not teach a liquid crystal display controller wherein the dithering pattern register section forms dithering patterns by dividing the gray levels into groups each having a same denominator value but Weise et al teach a system for displaying color on a computer using dithering techniques by dividing the area of the color display to be filled with an application–specified RGB value into 8-by-8 groups which would obviously make the denominator value to be 8 for all patterns (col. 4, lines 56-61).

It would have been obvious to one of ordinary skill in the art to utilize the dithering pattern techniques taught by Weise into the device of Ishii et al because it would a system and method for generating a dither pattern that is a close approximation of a specified color (col. 3, lines 8-10).

As per claim 3 Ishii et al teach a liquid crystal display controller wherein the dithering pattern register section is programmed to store the binary data as much as duty cycles for the respective gray levels using predetermined numbers as denominator values of the gray levels (col. 4, lines 11-17).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Cariffe (US 5,638,187) teach an image dithering method enabling conversion of a gray level pixel image into a binary pixel image.

Allowable Subject Matter

6. Claims 4-6 and 9-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

None of the references, either singularly or in combination, teaches or even suggest the totality of the combination of elements as follows:

As per claims 4-6, a liquid crystal display controller wherein each of the modular register counters comprises:

a modular frame counter for performing counting operation whenever a frame is changed in response to the frame clock;

a modular line counter for performing counting operation whenever a line of the frame is changed in response to the line clock;

a modular pixel counter for performing counting operation whenever a pixel of the line is changed in response to the pixel clock;

a next frame counter for generating a first update value to the modular frame counter in response to an output signal of the modular frame counter so that a current value in the modular frame counter is updated whenever the frame is changed;

a next line counter for generating a second update value in response to an output signal of the modular line counter;

a first multiplexer for selectively generating an initial value of the modular frame counter or the second update value provided from the next line counter to the modular line counter in response to a first selection signal;

a next pixel counter for generating a third update value whenever the pixel is changed in response to an output signal of the modular pixel counter; and

a second multiplexer for selectively generating the initial value of the modular frame counter, an initial value of the modular line counter, or the third update value provided from the next pixel counter to the modular pixel counter in response to a second selection signal.

As per claims 9-14, a method wherein the step of performing counting operation comprises the steps of:

performing counting operation whenever a frame is changed in response to the frame clock;

performing counting operation whenever a line of the frame is changed in response to the line clock;

performing counting operation whenever a pixel of the line is changed in response to the pixel clock;

providing a first update value whenever the frame is changed to update a current value for the counting operation in response to the frame clock;

providing a second update value whenever the line is changed in response to a result of the counting operation in response to the line clock;

selectively providing an initial value for the counting operation in response to the frame clock or the second update value, to update a current value for the counting operation in response to the line clock;

providing a third update value in response to a result of the counting operation in response to the pixel clock whenever the pixel is changed; and

selectively providing the initial value for the counting operation in response to the frame clock, an initial value for the counting operation in response to the line clock, or the third update value, to update a current value for the counting operation in response to the pixel clock.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald Laneau whose telephone number is 703-305-3973. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6.00 PM or via email: ronald.laneau@uspto.gov.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached at 703-305-4709.

8. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Ronald Laneau
Examiner
Art Unit 2674

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

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October 30, 2003